

Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) An application specific integrated circuit (ASIC) comprising:

a standard cell including a plurality of logic functions;

at least one bus coupled to at least a portion of the logic functions;

a plurality of internal signals from the plurality of logic functions; and

a field programmable gate array (FPGA) coupled to the at least one bus and the plurality of internal signals, the ~~field programmable gate array (FPGA)~~ including a debug client function that observes and manipulates the at least one bus and the plurality of internal signals, the debug client function being in communication with a network server and including

media access controller to provide communication with the network server over a network, including downloading information for a debugging session,

comparator logic operable to compare selected ones of the plurality of internal signals coupled to the ~~field programmable gate array (FPGA)~~ with a trigger pattern downloaded from the network server; and

storage logic operable to store a state of the selected ones of the plurality of internal signals that match the trigger pattern for later retrieval by the network server.

2. (Previously Presented) The ASIC of claim 1, wherein the at least one bus comprises an internal bus, the internal bus being internal to the ASIC and not being

exposed via an I/O pin.

3. (Currently Amended) The ASIC of claim 2, wherein the server comprises a ~~networked~~ network server running a debugger application.

4. (Currently Amended) The ASIC of claim 3, wherein the debug client function is programmed by the ~~networked~~ network server.

5. (Currently Amended) The ASIC of claim 1, wherein the debug client function further includes:

external communicator logic for receiving and transmitting information to the server;
selector logic coupled to the at least one bus and the plurality of internal signals, the selector logic to provide each one of the plurality of internal signals coupled to the ~~field programmable gate array (FPGA)~~ at a particular input point within the debug client function;
and

interface logic coupled between the external communicator logic and the selector logic for providing communication therebetween.

6. (Previously Presented) The ASIC of claim 5, wherein the interface logic comprises:
the storage logic;

the comparator logic, wherein the comparator logic is coupled to the storage logic;
and

output logic coupled to the comparator logic for controlling the plurality of internal signals on the ASIC.

7. (Previously Presented) The ASIC of claim 4, wherein the server utilizes the debug client function to debug hardware within at least one of the plurality of logic functions.

8. (Previously Presented) The ASIC of claim 4, wherein the server utilizes the debug client function to debug software within at least one of the plurality of logic functions.

9-22. (Cancelled)